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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,552	08/02/2003	Marcos Karnezos	CPAC 1017-5	2572

22470 7590 04/04/2005

HAYNES BEFFEL & WOLFELD LLP
P O BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,552	KARNEZOS, MARCOS	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 17 and 19 - 36* is/are pending in the application.

4a) Of the above claim(s) *20 - 34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 17, 19, 35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on January 10, 2005 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 5, 11, 12, 17, 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Ozawa et al. (U. S. Pat. No. 6,316,838).

Regarding claim 1, Ozawa et al. discloses in e.g., Fig. 6 a multi-package module comprising

- stacked first (21 and 33) and second packages (22 – 24),
- each said package including a die (23 and 21) attached to a substrate (24 and 33),
- wherein the first (33) and second (24) substrates are interconnected by wire bonding (32), and wherein the first package (21 and 33) comprises a flip-chip ball grid array package having a flip-chip (21) in a die-up configuration (see Fig. 6).

Regarding claim 2, Ozawa et al. discloses in e.g., Fig. 6 the second package (22 – 24) being a wire bonded land grid array package.

Regarding claim 3, Ozawa et al. discloses in e.g., Fig. 6 the die (23) and wire binds (31) in the second package being fully encapsulated with a molding material (26).

Regarding claim 4, Ozawa et al. discloses in e.g., Fig. 6 the second package (22 – 24) being peripherally encapsulated (26) to an extent sufficient to cover the wire bonds (31) between the die (23) and the substrate (24).

Regarding claim 5, since Ozawa et al. discloses in e.g., Fig. 6 the second package substrate (24) including a single metal layer (37), the element 37 on the second package substrate (24) reads as a single-metal layer substrate.

Regarding claim 11, Ozawa et al. discloses in e.g., Fig. 6 the second package (22 - 24) being a stacked die package.

Regarding claim 12, Ozawa et al. discloses in e.g., Fig. 6 adjacent stacked die (22 and 23) in the stacked die package (22 – 24) being separated by spacers (38).

Regarding claim 17, Ozawa et al. discloses in e.g., Fig. 6 at least one of the first and the second package being a stacked-die package.

Regarding claims 35 and 36, these claims merely recite the intended use or the environment in which the multi-package module of claim 1 is intended to be used. Since the claims fail to define any additional structure, Ozawa et al. anticipates these claims as well.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 – 10, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. in view of Kakimoto et al. (U. S. Pat. No. 6,333,552).

Regarding claims 6, 8, 10 and 13, while Ozawa et al. discloses in Fig. 6 the second package being stacked over the first package (claim 13) and the use of a chip in a flip chip package, Ozawa et al. does not appear to provide a specific type of the die to be an RF die (claim 8) and an electrical shield (claims 6, 10 and 13) in the first package. Kakimoto et al. teaches in e.g., Fig. 3 and column 1, line 56 – column 2, line 34 an electrical shield (57) and an RF die (30) in a flip chip package (the package in Fig. 7). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply the RF die as the specific type of the chip and the electrical shield in the structure of Ozawa et al. as taught by Kakimoto et al. to shield electromagnetic waves (column 1, lines 64 – 65).

Regarding claim 7, Ozawa et al. and Kakimoto et al. disclose the electrical shield (57) being a metal cap (column 1, lines 64 and 65). Inherently, every metal cap (57) dissipates heat from a chip. Thus, Ozawa et al. and Kakimoto et al. disclose the electrical shield (57) being configured to serve as a heat spreader.

Regarding claim 9, since Ozawa et al. and Kakimoto et al. disclose the electrical shield and the RF chip, Ozawa et al. and Kakimoto et al. disclose the following limitation "the flip chip

package includes an RF die, and the shield serves to limit electromagnetic interference between the RF die and other die in the multi-package module."

Regarding claim 19, since Ozawa et al. and Kakimoto et al. disclose a metal cap (57; column 1, lines 64 and 65). Inherently, every metal cap has a function of shielding any external heats from a chip. Thus, Ozawa et al. and Kakimoto et al. disclose a heat shield.

6. Claims 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa et al. in view of Lin (U. S. Pat. No. 5,436,203).

Regarding claim 14, while Ozawa et al. discloses in Fig. 6 the use of the first package substrate, Ozawa et al. does not appear to provide an embedded ground plane in the first package substrate. Lin teaches in e.g., Fig. 1 and column 6, lines 18 – 20 an embedded ground plane (22) in a package substrate (12). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply the embedded ground plane in the first package substrate of Ozawa et al. as taught by Lin to establish a shield surrounding semiconductor die which protects against either external or internal EMI (column 6, lines 18 – 22).

Regarding claim 15, since Ozawa et al. and Lin disclose the ground plane (22) being configured to serve for heat dissipation (column 6, lines 61 – 63 of Lin).

Regarding claim 16, since Ozawa et al. and Lin disclose the ground plane (22) being configured to serve as an electrical shield (column 6, lines 18 – 22 of Lin).

Response to Arguments

7. Applicant's arguments filed on January 10, 2005 have been fully considered but they are not persuasive.

On page 11, applicant argues that Ozawa does not describe each said package including a die attached to a substrate. That is, the first package has at least one die attached to a first package substrate, and the second package has at least one die attached to a second package substrate. Thus, the rejection of claim 1 as anticipated by Ozawa should be withdrawn. This argument is not persuasive. First, the term "substrate" is a broad term and in light of its breadth, the element (24) in Fig. 6 of Ozawa is considered to be a "substrate" for the chip (23) in the second package. Since Ozawa provides a second substrate in the physical arrangement as claimed, it is considered to meet the structural limitations of the claims and the argument is not persuasive.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Monday, March 28, 2005

GEORGE ECKERT
PRIMARY EXAMINER